Integrity ★ Service ★ Excellence

Update on SET Reliability Project

18 Jun 2014

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Space Electronics Technology
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Outline of Talk

- Background
- Our Focus
- Fundamental Research
  - N/PBTI Research
  - Potential Trust Application
  - Modeling NBTI
- Applied Research
  - Temperature Behavior of NBTI & HCI
  - JNT Demo/Eval
- Future Plans
- Summary

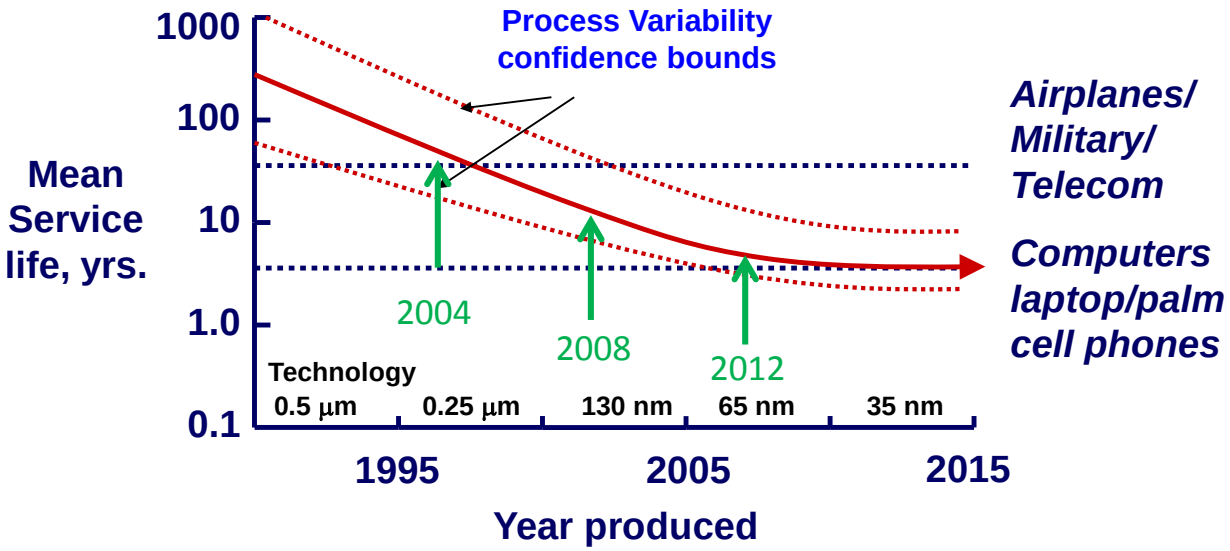
Reliability Research Group

Rod Devine	Think Strategically	Lead, Experimenter
Ken Kambour	LEIDOS	Modeling
Ed Gonzales	Think Strategically	Process Engineer
Duc Nguyen*	COSMIAC	Graduate UNM
Camron Kouhestani	COSMIAC	Graduate UNM

* Started work at Sandia on 1 Jun 14

Reliability of modern electronics less than satellite mission life

- **As IC feature size decreases, average IC lifetime decreases**



From:
State of the Art Semiconductor Devices in Future Aerospace Systems
L. Condra, Boeing, J. Qin and J.B. Bernstein, U of Maryland 2007

Reliability is maintained in RH devices in many ways including by reducing performance to well below that of related commercial devices—1995 Motorola PPC750 was 366 MHz, 2003 Rad 750 was 133 MHz (.26μ vs .25μ)

Note: between 1997 and 2008 the service lifetime decreased by 10 x

Note – $MTTF_{IC} = (\sum^{n}_{i=1} \lambda_i)^{-1}$ where λ_n = degradation rate for mechanism i and n is the number of mechanisms in the IC

Many (Especially in Government) are Increasingly Concerned About Reliability…

Government Microcircuit Applications and Critical Technologies Conference 2014

Conference Theme: *Reliability, Remembering the Recipe*

NIST-Sponsored Workshop (2014): *Resilient, Robust, Reliable Electronic Materials and Devices Beyond Silicon*

As the end of silicon scaling approaches, new materials are being exploited…High-K (Hf based) gate dielectrics and metal gates are already in use…finally device-level quality has been obtained but their reliability issues are largely unexplored. In addition, the geometry of the basic planar device is being changed – FINFET's, gate all around (nanowire)…

Taking this all together, it means lifetime prediction of new devices is extremely difficult. … Generally, parts are qualified by accelerated testing. …accurate prediction of lifetime requires accurate models of the underlying physical mechanisms.

We've focused on NBTI mechanisms for advanced space electronics

…but Industry is Not

Reliability: fallacy or reality?
Gonzalez, A. (INTEL)(Univ. Polytech. de Catalunya, Barcelona, Spain); Mahlke, S.; Mukherjee, S.;(INTEL) Sendag, R.; Chiou, D.; Yi, J.J.(Freescale)
Source: *IEEE Micro*, v 27, n 6, p 36-45, Nov.-Dec. 2007

But, the majority of **consumers care little about the reliable operation** of electronic devices, and their concerns are decreasing as these devices become more disposable. In 2006, the average lifetime of a business cell phone was nine months. The average lifetimes of a desktop and a laptop computer were about two years and one year, respectively…….. **Therefore, building devices whose hardware functions flawlessly for 20 years is simply unnecessary.**

Gonza´lez: **Any idea on how we can measure reliability?**
Mukherjee: We fundamentally need a mechanism to measure these things. For hard errors, the problem may be tractable. For soft errors—induced by radiation—this is still a hard problem. **For gradual errors, such as wear-out, we still don't know how to measure the reliability of an individual part**. So, the answer is that, in many cases, we don't know how to measure reliability.

Industry will not attempt to provide lifetimes required for space applications

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Our Focus

- **NBTI, HCI, & EM dominate failure mechanisms in sub-45nm ICs**
  - **We focus on NBTI and HCI since HiREV has others working EM**
- **Fundamental research**
  - **Identify physics of failure responsible for N/PBTI**
  - **Model time-dependent behavior of N/PBTI in circuits**
  - **Investigate synergy of radiation and reliability mechanisms**
  - **Identify physics of failure responsible for HCI**
- **Applied Research**
  - **Explore new device types with improved intrinsic reliability**
    - **Currently, the Junctionless Nanowire Transistor (JNT)**
- **Collaborate with colleagues**
  - **Develop measurement protocols that accelerate reliability testing and yield accurate results**
  - **Collaboration with multiple research establishments: NRL, SEMATECH, HIREV, Ariel U, Sandia, CINT, DMEA, …**

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Fundamental Research

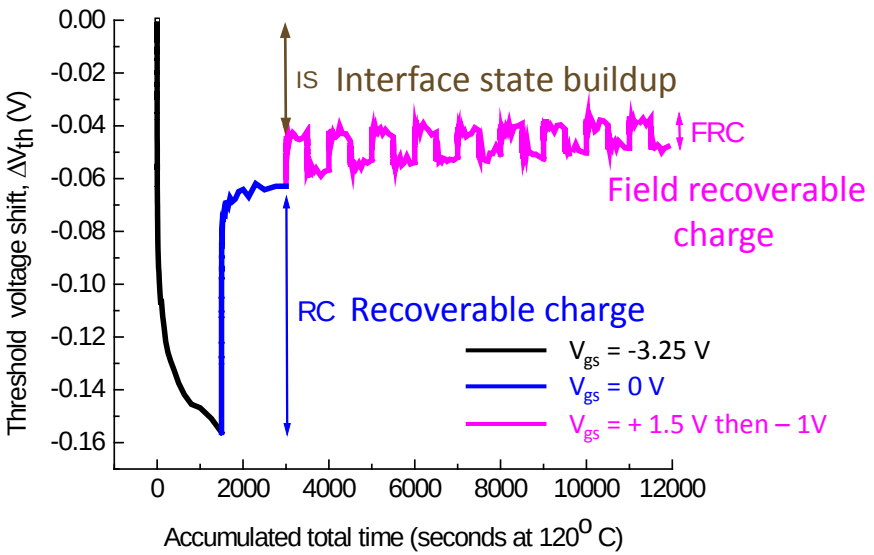
- **Expanded research into NBTI and PBTI in 130 nm and 90 nm devices with SiON gate dielectrics**
- **Began NBTI research on 32 nm high-k gate dielectric (HfO_2/SiO_2) PMOS devices**
  - **Observed RC and FRC trapped charges with less IS**
  - **Establishing electric field and temperature dependencies**
- **Evaluating comparative reliability of SiON and high-k gate dielectric devices**
- **Began initial investigation of methods to evaluate complex circuit reliability based on individual device response**

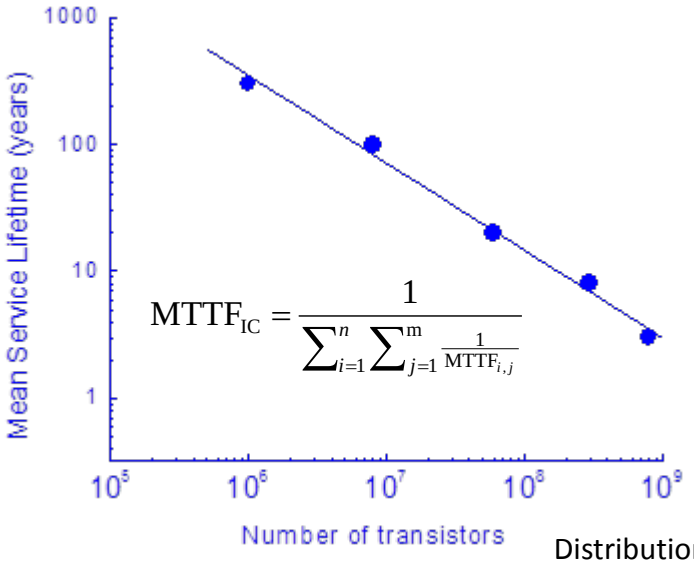
RC: Recoverable Charge
FRC: Field Recoverable Charge
IS: Interface State

Previously Published
Our Measurements Reveal the Multi-Defect Origin of NBTI

- **We have developed a *unique* measurement protocol enabling extraction of the time dependence of degradation components based upon continuous & pulsed stressing**
  - **This is essential for incorporation into long-term reliability models**
  - **Now know several defects types are responsible for NBTI**

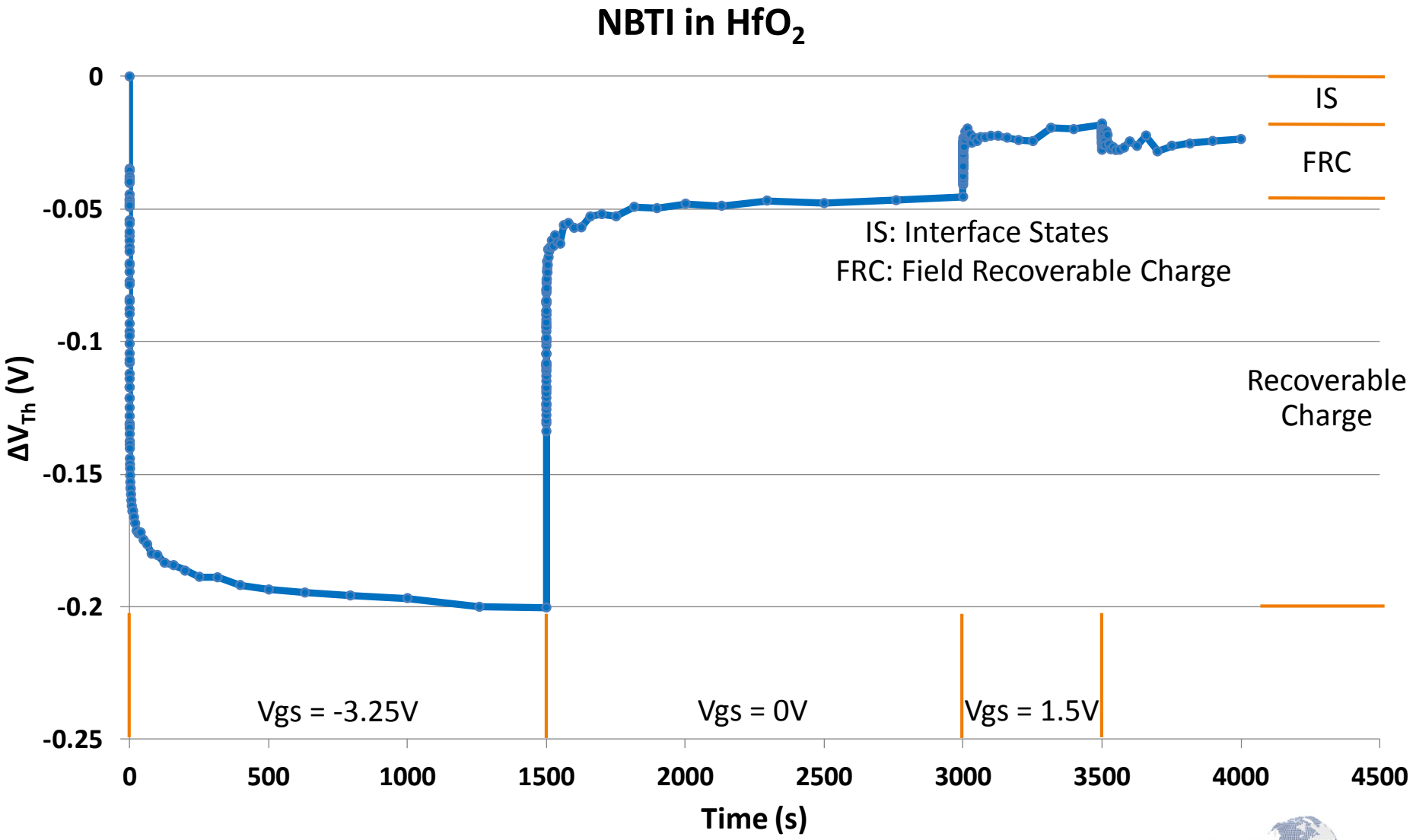
Interface : Si-H + $h^+ \rightarrow Si^+ + H$ or $1/2H_2$
Insulator "bulk": $X_1 + h^+ \leftrightarrows X_1^+$
Insulator "bulk": $X_2 + h^+ \rightarrow X_2^+ \leftrightarrows Y$



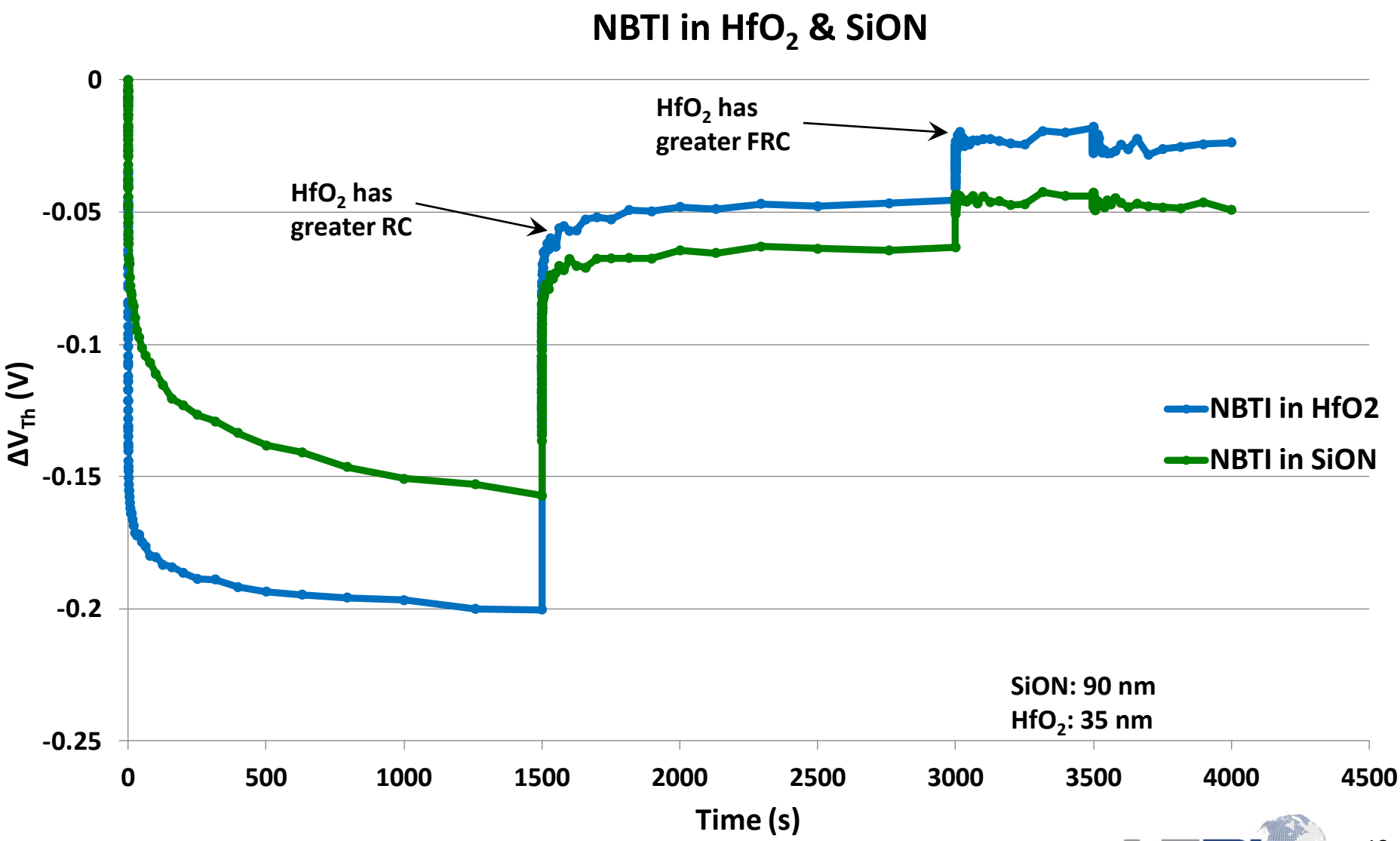


- **Used protocol to measure lifetime characteristics of various transistors**
  - **Findings: Contrary to widely held hypothesis, increasing number of transistors in an IC contributes more to reduced lifetime than change in transistor reliability**

Our NBTI Measurements

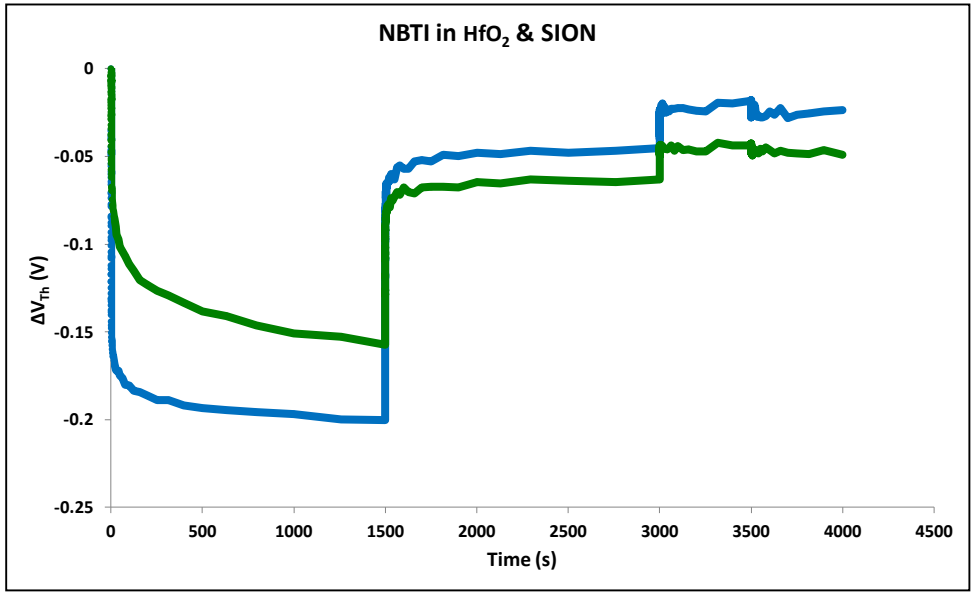


Our NBTI Measurements



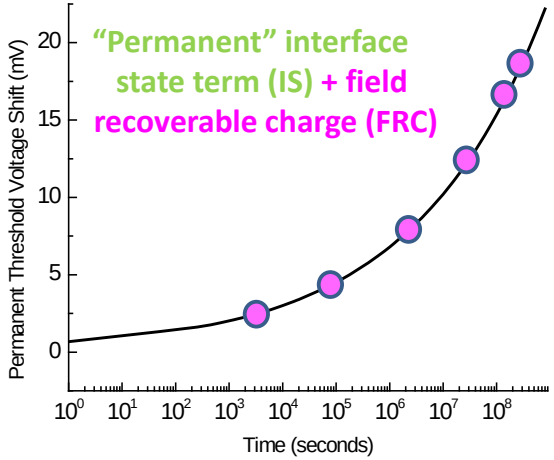
Potential Trust Applications

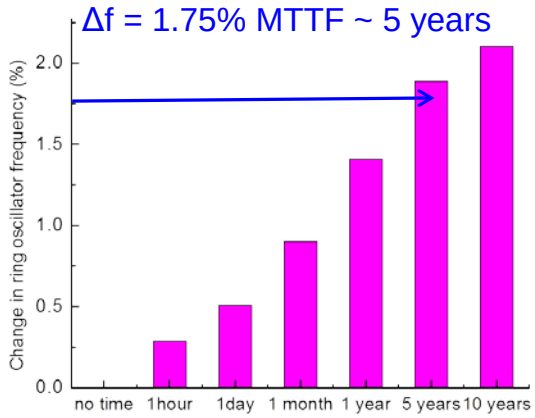
- **Can NBTI characteristics of a device be used in fingerprinting an IC?**
  - **NBTI characteristics are determined by a combination of the manufacturing process and the transistor design**
  - **We expect they are "impossible" to duplicate**



Reliability Modeling

- **Have taken first steps in developing lifetime modeling capability for complex circuits**
- **Model based on simple measurements to estimate device lifetime**
  - **Use high-temp to accelerate ΔV_{Th}**
  - **Use circuit simulation to measure the effect of permanent change in threshold voltage on a ring oscillator**
  - **When oscillator operation goes outside of circuit spec, device has failed**
- **Validation of model in process**





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Distinct HCI & NBTI Mechanisms

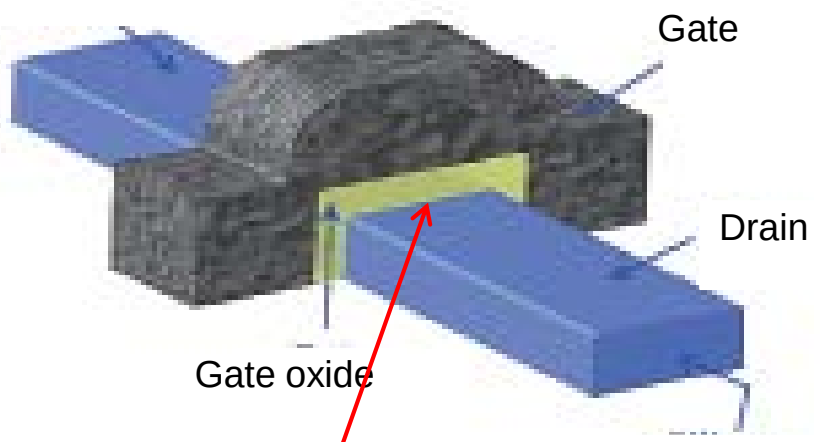
- Work by Dr. Joe Bernstein of Ariel University
- Data from Xilinx Spartan 6
  - 45nm commercial device
  - 21 Stage ring oscillator
- At -35C HCI dominates the degradation
- At +140C NBTI dominates the degradation
- Current lifetime estimates require single dominant mechanism across the temperature range

Fundamentally challenges lifetime analysis methods

The JNT—How does it work?

Several organizations are working on Junctionless Nanowire Transistors (JNTs) but their focus in optimizing design

Structure is reminiscent of the FINFET but it's just an illusion !



In a MOSFET, NBTI degradation results from charge injection from the Si into the gate dielectric

The work function difference between the heavily doped wire and the gate electrode creates a field which depletes the wire under the gate → conductivity = 0

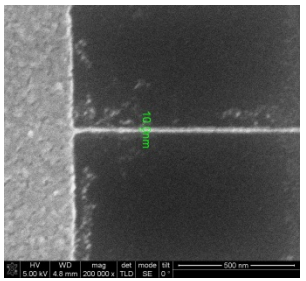
Apply a compensating potential: field → 0 wire is uniform conductor.

Note: when there is a field there are no charges in the wire. when there are charges, there's no field.

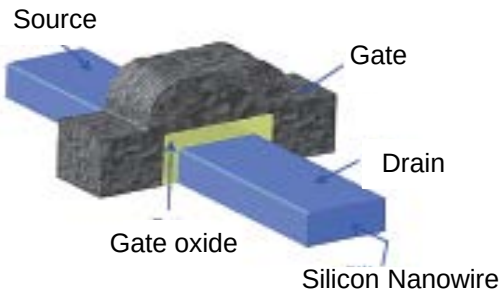
Hypothesis: JNT Eliminates NBTI, HCI, TDDB, …
No Field, No Charge, No Reliability Issues

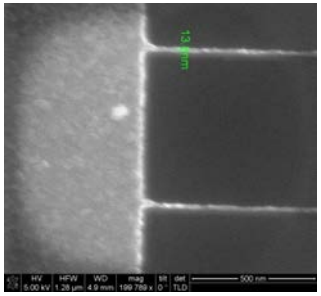
Junctionless Nanowire Transistor

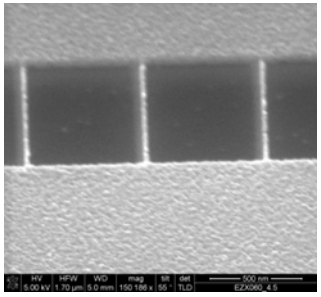
- **Concentrated on building Junctionless Nanowire Transistors (JNTs)**
  - **Developed 27 step process flow.**
  - **Performed e-beam lithography at Center for Integrated Nano Technologies (DOE)**



No Gate, 10nm wire







Multiple Wires in Parallel for Current Reqirements

Target Si thickness = 10 nm
Target gate oxide = 3 nm
Target channel length ≤ 1 μm

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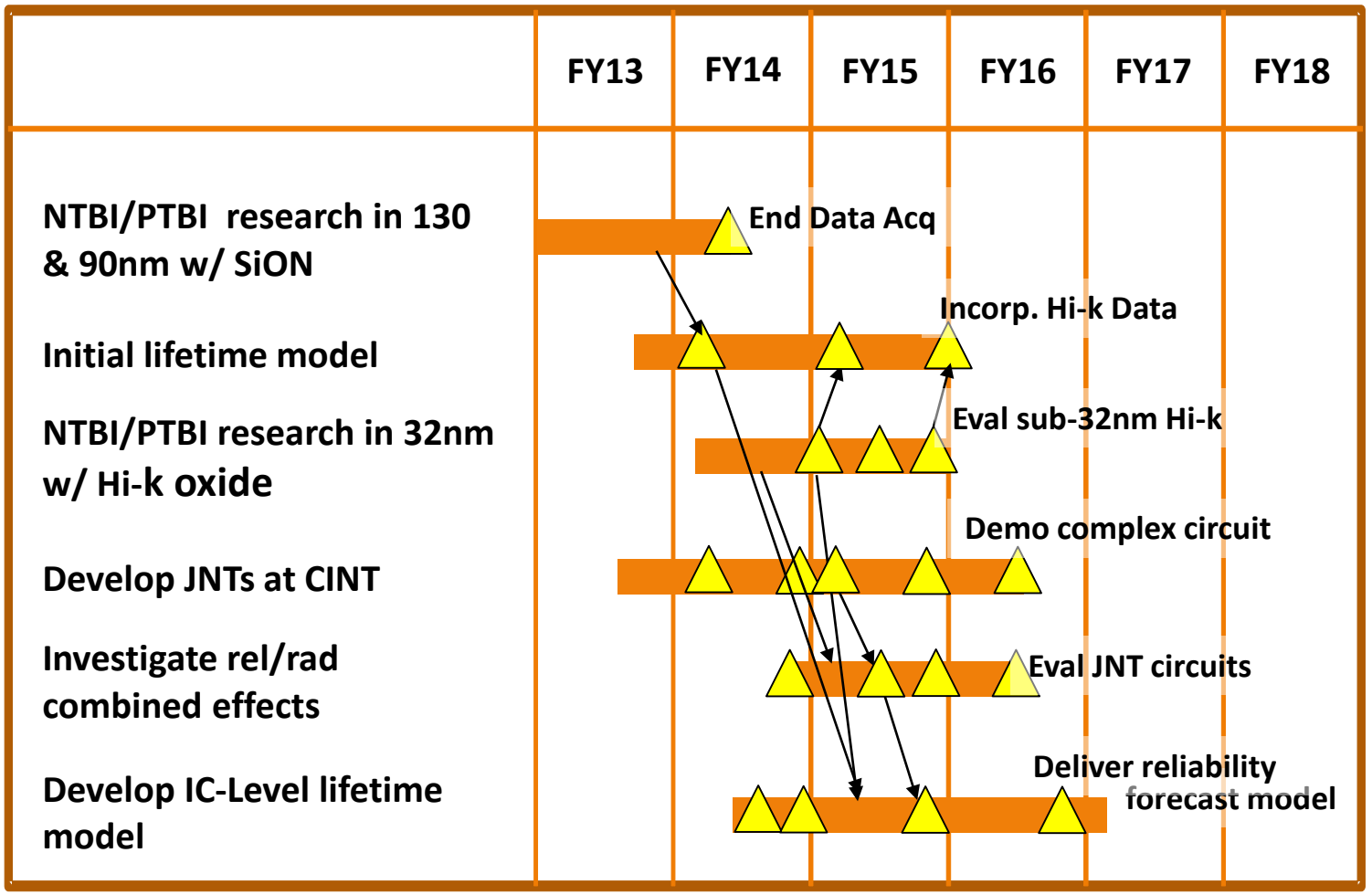
Near and Medium Term Plans

- **Basic research**
  - **Continue evaluating single-device reliability as technology evolves**
    - **Is device-level reliability constant or does it degrade with generation?**
  - **Continue modeling how single-device reliability affects circuit response (in house)**
  - **Develop "black box" circuit reliability evaluation (contract)**
  - **Determine if radiation changes reliability**
    - **They have similar mechanisms**
- **Applied Research**
  - **Reproducibly build JNTs and evaluate rad & rel hardness**
    - **Build and evaluate small circuits such as NAND gates, etc**
    - **Determine feasibility of 3D JNT circuits**

Roadmap



Summary

- **AFRL Space Electronics Technology Program has focused on a few aspects of reliability in deep-submicron ICs**
  - **Basic mechanisms responsible for NBTI/PBTI**
  - **Combined effects of radiation and NBTI**
  - **Basic mechanisms responsible for HCI and combined effects**
  - **Black-box approach to forecasting IC lifetime**
  - **Evaluation of Junctionless Nanowire Tranistors**
    - **Expect immunity to radiation, NBTI, etc.**

Questions?

Backup Charts

Pubs Since 1 Oct 13

Published presentations at conferences (in Proceedings)

- Electrochemical Society – San Francisco 2013 — 2 papers
- Electrochemical Society – Orlando 2014 — 1 paper
- International Integrated Reliability Workshop 2013 — 2 papers
- MRQW December 2013 (invited) — 1 pres't

Journal publication

- Journal of the Vacuum Science & Technology B — 1 paper

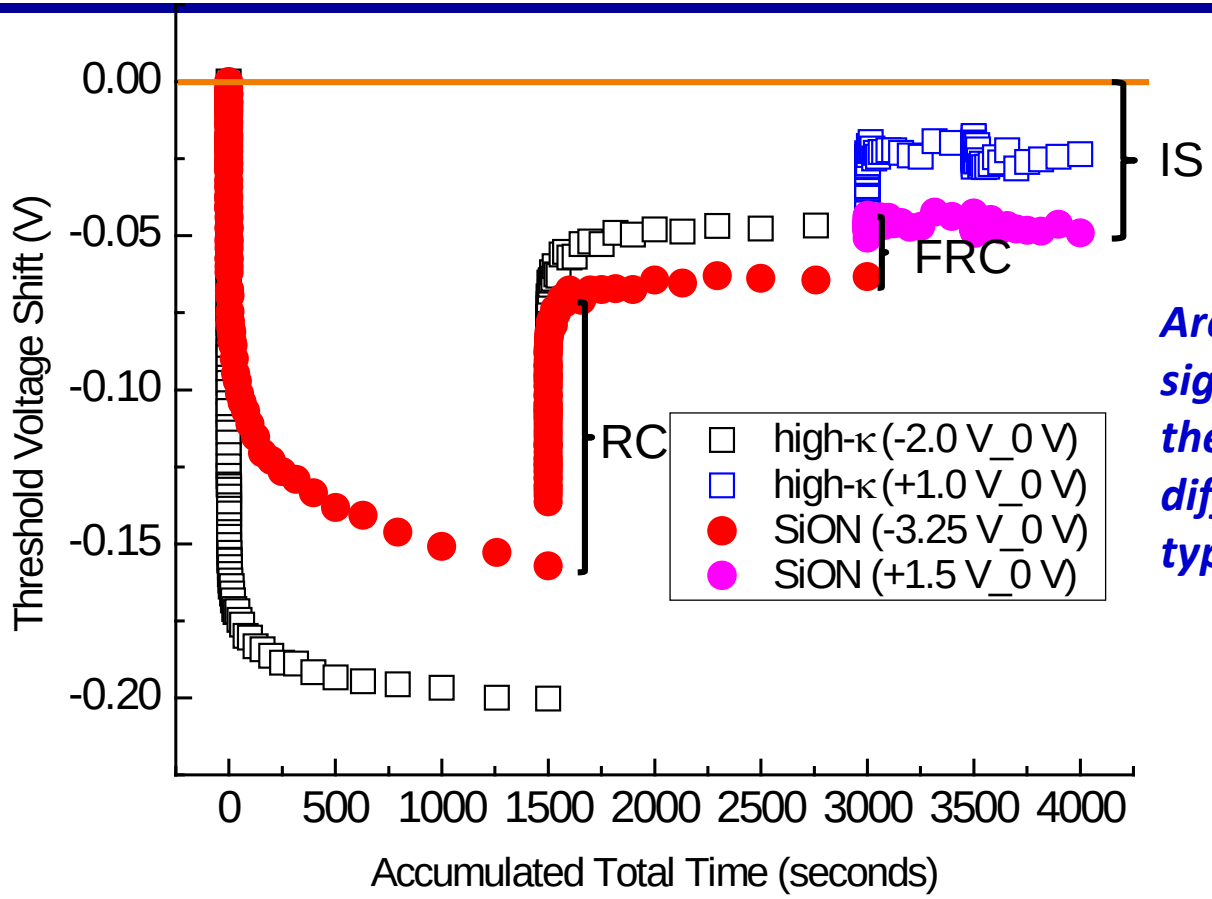
Thesis

- Master's Thesis with distinction, Duc Nguyen, Dec 2013
- Master's Thesis with distinction, Camron Kouhestani, May 2014

Reliability Project Milestones

Topic	Timeline	Action
130 nm/90 nm	Q2 FY 14	End data acquisition cycle
Initial lifetime model	Q2 FY 14	transfer 130/90 nm data
	Q2 FY 15	transfer prelim. High k data
	Q4 FY 15	transfer advanced high k data
High k	Q4 FY 14	Data transfer to initial lifetime model
	Q2 FY 15	Measurements on devices < 32 nm channel
	Q4 FY 15	Data transfer to initial lifetime model
JNT	Q2 FY 14	1st P type JNT prototype
	Q4 FY 14	Device characterization complete
	Q2 FY 15	1st N type JNT prototype
	Q4 FY 15	Device characterization complete
	Q2 FY 16	Simple circuit (inverter)
	Q2 FY 17	Complex circuit (multistage ring oscillator)
Rad/Rel effects	Q4 FY 14	Experimental set-up determined
	Q2 FY15	Test first short channel devices
	Q4 FY 15	Test first JNTl devices
	Q2 FY 16	Test new FETs
IC level modeling	Q2 FY 14	First data on complex circuit
	Q4 FY 14	Confront complex circuit results with results of single device analysis
	Q4 FY15	Confront complex circuit results with results of single device analysis
		using rad hard technology
	Q4 FY 16	Develop accurate long term reliability prediction protocol

Comparison of SiON/HfO_2 data



Are these differences significant relative to the device-to-device differences of a single type?

RC: Recoverable Charge
FRC: Field Recoverable Charge
IS: Interface State

Potential Trust Application

- **Hypothesis: NBTI characteristics of a device can be used to fingerprint ICs**
- **The characteristics are determined by a combination of the manufacturing process and the transistor design—it is likely they are impossible to duplicate in another foundry**